Annex no.1

Request for Proposal no. 03/2016

Technical Specification

Line	Item	Item Description	Quantity
1	IP core suite with sources	IP core suite for 7. generation of Xilinx FPGA, in particular Zynq family for IEEE1588-2008 v2 (PTPv2) clock synchronization with FPGA hardware assist. The solution must be able to use GMII connection available in Zynq-7 family as well as PS GMAC Ethernet path. The solution must be compatible with Xilinx Vivado version 15.4 and support gigabit Ethernet. The IP core must have at least 64bit PTP timer that is accessible through FPGA logic. The IP core must have PPS (Pulse Per Second) output. The IP core must support PTPv2 in both, second and third layer of network interfaces. The IP core must be able to use timestamps on incoming and outgoing frames. The solution must be able to use both, Peer-to-Peer and End-to-End clocks. The solution should be optimized for minimum FPGA resource utilization. The solution should provide accuracy of time synchronization (measured as the difference between PPS outputs of FPGA and PTP Master) better than +/- 100ns. The sources with HDL must be included.	1
2	Software for Linux	The software for the Linux platform for PTPv2 packets processing in association with dedicated IP core (described in 1st pos.) The software must provide access to the timestamp inside the FPGA and the Best Master Clock (BMC) selection algorithm. The software must be compatible with the Petalinux Linux version 15.4 distribution for Zynq family provided by Xilinx.	1
3	Reference Project	The reference project for Zynq platform and Linux Operating System allowing the use of the IP Core in PTPv2 time synchronization. The supplier must provide support during the design implementation on chosen platform.	1