Annex no. 1

for the inquiry no 7/eCAUSIS/2023

Technical parameters

Order subject:
Complete IP block implementing 10/25Gbps Ethernet

CPV code: 48000000 - Software packages and information systems

Brief description of the device:
The subject of the order is a complete IP block implementing 10/25 Gbps Ethernet at RTL level. The IP block should comply with IEEE 802.3 Clause 49, IEEE 802.3by and should include PCS, PMA and MAC sublayers. The solution should be compatible with Xilinx Vivado environment and Xilinx FPGAs.

General requirements:

1. Complete IP block designed to meet the requirements of 10/25Gbps Ethernet as defined by the IEEE 802.3 Clause 49 specification, IEEE 802.3by
2. Implements complete Ethernet MAC and PCS/PMA
3. User-selectable baud rate, auto-negotiation not required. Transmission speed switchable during operation.
4. The IP block should be supplied together with a wrapper suitable for instantiation in a Vivado environment, a netlist, sample test scripts, compilation scripts and Linux-compatible drivers.
5. IP design files should be provided in the form of any RTL-level hardware description language.
6. The IP block should provide information on the status of the connection and collect statistics on that connection.
7. AXI4-Stream user interface required
8. Systems families supported:
    a. Kintex UltraScale
    b. Artix UltraScale+
    c. Virtex UltraScale+
    d. Kintex UltraScale+
    e. Zynq UltraScale+™ MPSoC
    f. Zynq UltraScale+™ RFSoC
    g. Versal ACAP
9. Compatibility with Vivado 2020.1 and later
10. Technical support and availability of updates for at least 1 year from the date of purchase

Detailed features:
Optional features:
- On-site licence